520.43578X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: AKITA

Serial No.:

Filed: March 3, 2004

For: Logic Circuit And Program For Executing Thereon

Group:

Examiner:

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 & 1.98

Mail Stop: DD
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

March 3, 2004

Sir:

In the matter of the above-identified application, applicant is submitting herewith copies of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted within three months of the filing date.

Each of the documents listed on the attached form equivalent to Form PTO-1449 is in the English language.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry,

Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case: 520.43578X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

Alan E. Schiavelli
Registration No. 32,087

AES/jla
(703) 312-6600
Attachments

FORM PTO-1449 (Rev. 4/92) U.S. Department of Commerce Patent and Trademark Office

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
520.43578X00	
APPLICANT: AKITA	
FILING DATE: March 3, 2004	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		Sohi, G.S., "Instruction Issue Logic For High-Performance, Interruptible, Multiple Functional Unit, Pipeline Computers, IEEE Transactions on Computers, Vol. 39, No. 3, March 1990, pp 349-359
		Fisher, J.A., "Very Long Instruction Word Architectures and ELI-512" Proceedings of the 10th International Symposium on Computer Architecture 1983
		R. Hartenstein, " Coarse Grain Reconfigurable Architectures", ASP-DAC 2001, pp 564-569

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation is considered, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.